Bumping Process at Amkor Taiwan (AT5) and Flip Chip CSP_BGA at SK3 Qualification

QUALIFICATION PLAN			
TEST	**SPECIFICATION**	**SAMPLE SIZE**	**RESULTS**
Temperature Cycle (TC)*	JEDEC *JESD22-A104*	3 x 32	**PASS**
Unbiased Highly Accelerated Stress Test (uHAST)*	JEDEC *JESD22-A118*	3 x 32	**PASS**
Solder Heat Resistance (SHR)*	JEDEC/IPC *J-STD-020*	3 x 11	**PASS**
Electrostatic Discharge *Field Induced Charge Device Model*	JEDEC *JESD22-C101*	3/voltage	**PASS ±250V**

*Preconditioned per JEDEC/IPC J-STD-020